TITLE OF THE INVENTION

POWER-ON DETECTOR, AND POWER-ON RESET CIRCUIT USING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2003-096691, filed March 31, 2003, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power-on detector which detects power-on in a semiconductor integrated circuit device or the like, and a power-on reset circuit which initializes a register or latch circuit upon power-on.

2. Description of the Related Art

A conventional power-on detector is constituted by series-connecting a resistor and a diode or diode-connected transistor, and connecting the connection node to the input terminal of an inverter. The power-on detector generates a power-on detection signal by utilizing the fact that an output from the inverter is inverted as the power supply voltage rises upon power-on.

FIG. 1 is a circuit diagram showing an arrangement example of such conventional power-on detector.

The source of a p-channel MOS transistor 11 is connected to a power supply V_{DD}, and the drain and gate are connected to one terminal of a resistor 12. The other terminal of the resistor 12 is connected to ground V_{SS}. The connection node between the drain of the MOS transistor 11 and one terminal of the resistor 12 is connected to the input terminal of a CMOS inverter 15 comprised of a p-channel MOS transistor 13 and n-channel MOS transistor 14. A power-on detection signal PDS is output from the output terminal of the CMOS inverter 15.

In this arrangement, when the semiconductor integrated circuit device is powered on, the potential of the power supply V_{DD} increases. When the potential of the power supply V_{DD} reaches a circuit operable level, the potential at the connection node between the diode-connected MOS transistor 11 and resistor 12 becomes higher than the circuit threshold voltage of the CMOS inverter 15. As a result, the output voltage (power-on detection signal PDS) of the CMOS inverter 15 changes to low level ("L" level). The potential of the power supply V_{DD} further increases. When the potential at the connection node between the MOS transistor 11 and the resistor 12 becomes lower than the circuit threshold voltage of the CMOS inverter 15, the output voltage of the CMOS inverter 15 is inverted to high level ("H" level), and power-on is detected.

The power-on detection level can be controlled by adjusting the resistance value of the resistor 12 or the channel length/channel width ratio (L/W) of each of the MOS transistors 11, 13, and 14.

A technique of detecting power-on by the output signal PDS from the CMOS inverter 15 via a noise-cut low-pass filter (LPF) has also been known. The use of the low-pass filter can enhance noise resistance.

In the above-mentioned arrangement, however, the power-on detection level varies upon a change in temperature condition or variations in manufacturing process. This may result in a defective chip. For example, an onboard semiconductor integrated circuit device must normally operate within a wide temperature range of -40℃ to +125℃. A great change in temperature condition changes the threshold voltages of the MOS transistors 11, 13, and 14. The level at which the power-on detection signal PDS is inverted greatly varies. The resistor 12 is generally a diffused resistor. The resistance value of the diffused resistor readily varies upon variations in manufacturing process. Such variations cannot be fully coped with by adjusting the resistance value of the resistor 12 or the channel length/channel width ratio of each of the MOS transistors 11, 13, and 14.

When a semiconductor integrated circuit device incorporates a low-voltage circuit which operates

around 1 V, the influence of a change in temperature difference or variations in manufacturing becomes more prominent. It becomes difficult to detect power-on.

To solve this problem, a technique of detecting power-on by using a circuit with low temperature dependency, such as a band gap reference circuit is proposed (see, e.g., Jpn. Pat. Appln KOKAI Publication Nos. 2002-43917 and H10-207580). However, no prior art can sufficiently reduce temperature dependency because an output voltage from the band gap reference circuit and a voltage prepared by resistance-dividing a power supply voltage are compared, in other words, a voltage free from temperature dependency and a voltage with temperature dependency (though temperature dependency is relatively low) are compared. Such technique is not satisfactorily applied to an onboard semiconductor integrated circuit device which is used under strict conditions.

The same problem occurs when a power-on reset circuit for initializing a register or latch circuit in a semiconductor integrated circuit device upon power-on is constituted using the above-described power-on detector. Demands have arisen for a measure against this problem.

BRIEF SUMMARY OF THE INVENTION

According to one aspect of the present invention, there is provided a power-on detector comprising

a reference potential generation circuit which generates a reference potential, and a first comparator which compares a first voltage generated on the basis of the reference potential output from the reference potential generation circuit and a potential of a first potential supply source, and a second voltage generated on the basis of the reference potential and a potential of a second potential supply source different from the potential of the first potential supply source, wherein power-on is detected when a potential difference between the potentials of the first and second potential supply sources upon power-on becomes larger than a sum of the first and second voltages.

According to another aspect of the present invention, there is provided a power-on reset circuit comprising a data holding circuit which holds data, a reference potential generation circuit which generates a reference potential, a first comparator which compares a first voltage generated on the basis of the reference potential output from the reference potential generation circuit and a potential of a first potential supply source, and a second voltage generated on the basis of the reference potential and a potential of a second potential supply source different from the potential of the first potential supply source, and a reset circuit which resets data held by the data holding circuit on the basis of an output signal from

the first comparator, wherein the reset circuit resets data held by the data holding circuit when a potential difference between the potentials of the first and second potential supply sources upon power-on becomes larger than a sum of the first and second voltages.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

FIG. 1 is a circuit diagram showing a conventional power-on detector;

FIG. 2 is a conceptual view for explaining a power-on detector and power-on reset circuit according to the first embodiment of the present invention;

FIG. 3 is a circuit diagram showing an arrangement example of the first circuit unit in the circuit shown in FIG. 2;

FIG. 4 is a circuit diagram showing an arrangement example of the second circuit unit in the circuit shown in FIG. 2;

FIG. 5 is a circuit diagram showing an arrangement example of the third circuit unit in the circuit shown in FIG. 2;

FIG. 6 is a circuit diagram showing a potential comparison circuit using a current source and current mirror circuit as an extracted part of the circuit shown in FIG. 2;

FIG. 7 is a circuit diagram showing an arrangement example of a comparator in the circuits shown in FIGS. 2, 3, 4, and 6;

FIG. 8 is a circuit diagram showing a circuit, e.g., latch circuit which is reset by the detection signal of the power-on detector shown in FIGS. 2 to 7;

FIG. 9 is a waveform chart showing changes along the time axis in the potential of a power supply upon power-on, the level of a power-on detection signal, and a voltage input to the comparator; and

FIG. 10 is a circuit diagram for explaining a power-on detector and power-on reset circuit according to the second embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 is a conceptual view for explaining a power-on detector and power-on reset circuit according to the first embodiment of the present invention.

A BGR (Band Gap Reference) circuit 20 is a reference potential generation circuit which generates a reference potential with low temperature dependency. The BGR circuit 20 is comprised of first, second, and third circuit units 21, 22, and 23. The circuit unit 21 is a circuit which generates a current ($dI/dT > 0$) having a positive temperature characteristic. The circuit unit 22 is a circuit which generates a current ($dI/dT < 0$) having a negative temperature characteristic. The output currents of the circuit units 21 and 22 are added by the circuit unit 23. As a result, the temperature characteristics of the circuit units 21 and 22 are canceled, and a current

(dI/dT + dI/dT = 0) substantially free from temperature dependency is generated.

The output current of the circuit unit 23 is supplied to a resistor 24 to generate a voltage (first voltage) V1. This output current is also supplied to a current mirror circuit 25. The current mirror circuit 25 supplies a current equal to the output current to a resistor 26, generating a voltage (second voltage) V2. The voltage V1 becomes substantially free from the temperature characteristic with respect to the potential of ground V_{SS} (potential of the first potential supply source). The voltage V2 becomes substantially free from the temperature characteristic with respect to the potential of a power supply V_{DD} (potential of the second potential supply source).

The voltages V1 and V2 are compared by a comparator (first comparator) 27 to output a power-on detection signal PDS. When the sum of a voltage applied across the resistor 26 and a voltage applied across the resistor 24 exceeds the voltages of the power supplies V_{DD} and V_{SS}, the comparator 27 changes the level of the power-on detection signal PDS from the potential of ground V_{SS} to that of the power supply V_{DD}. The voltages across the resistors 24 and 26 are substantially free from temperature dependency, as described above. The potential to which an output (power-on detection signal PDS) from the comparator 27

changes is not influenced by any temperature change.

If the power-on detection signal PDS output from the comparator 27 is used to generate a reset signal for a data holding circuit such as a register or latch circuit, a power-on reset circuit free from any influence of a temperature change can be constituted.

FIG. 3 shows an arrangement example of the circuit unit 21 in the circuit shown in FIG. 2. This circuit comprises a differential amplifier (comparator) 31 for generating a positive temperature characteristic, p-channel MOS transistors 32 and 33, a resistor 34, and diodes 35 and 36. The source of the MOS transistor 32 is connected to the power supply V_{DD}; its drain, to the non-inverting input terminal (+) of the comparator 31; and its gate, to the output terminal of the comparator 31. The source of the MOS transistor 33 is connected to the power supply V_{DD}; its drain, to the inverting input terminal (-) of the comparator 31; and its gate, to the output terminal of the comparator 31. The drain of the MOS transistor 32 is connected to one terminal of the resistor 34. The anode-cathode path of the diode 35 is connected between the other terminal of the resistor 34 and ground V_{SS}. The drain of the MOS transistor 33 is connected to the anode of the diode 36, and the cathode of the diode 36 is connected to ground V_{SS}. The diode 35 is larger in size than the diode 36. A voltage V_{OUTA} controlling a positive

temperature characteristic current is output from an output terminal 37 connected to the output terminal of the comparator 31.

FIG. 4 shows an arrangement example of the circuit unit 22 in the circuit shown in FIG. 2. This circuit comprises a differential amplifier (comparator) 41 for generating a negative temperature characteristic, p-channel MOS transistors 42 and 43, a diode 44, and a resistor 45. The source of the MOS transistor 42 is connected to the power supply V_{DD}; and its drain, to the inverting input terminal (-) of the comparator 41. The gate of the MOS transistor 42 receives the output voltage V_{OUTA} of the circuit unit 21. The anode of the diode 44 is connected to the drain of the MOS transistor 42; and its cathode, to ground V_{SS}. The diode 44 is equal in size to the diode 36. The source of the MOS transistor 43 is connected to the power supply V_{DD}; its drain, to the non-inverting input terminal (+) of the comparator 41; and its gate, to the output terminal of the comparator 41. One terminal of the resistor 45 is connected to the drain of the MOS transistor 43; and the other terminal, to ground V_{SS}. A voltage V_{OUTB} controlling a negative temperature characteristic current is output from an output terminal 46 connected to the output terminal of the comparator 41.

FIG. 5 shows an arrangement example of the circuit

unit 23 in the circuit shown in FIG. 2. This circuit comprises p-channel MOS transistors 51 and 52, and a resistor 53. The source of the MOS transistor 51 is connected to the power supply V_{DD}, and its gate receives the output voltage V_{OUTA} of the circuit unit 21. The source of the MOS transistor 52 is connected to the power supply V_{DD}, its drain is commonly connected to the drain of the MOS transistor 51, and its gate receives the output voltage V_{OUTB} of the circuit unit 22. The MOS transistors 51 and 52 operate as a current source circuit which extracts a current free from any temperature characteristic from outputs from the differential amplifiers 31 and 41. One terminal of the resistor 53 is connected to the common drain connection node between the MOS transistors 51 and 52; and the other terminal, to ground V_{SS}. A potential V_{REFDC} (reference potential) which is generated by adding the output currents of the circuit units 21 and 22 and is free from temperature dependency is output from an output terminal 54 connected to the common drain connection node between the MOS transistors 51 and 52.

The temperature dependency can be changed by adjusting the resistance values of the resistors 34 and 45. In this circuit, the resistance values are so adjusted as to reduce the temperature characteristic of the potential V_{REFDC} (reference potential).

The reference potential V_{REFDC} can be set by the resistance value of the resistor 53. The reference potential V_{REFDC} can be set high by increasing the resistance value of the resistor 53, and low by decreasing the resistance value. The use of a variable resistor 53 allows freely setting the reference potential V_{REFDC}.

FIG. 6 shows an extracted part of the circuit shown in FIG. 2. This circuit is a potential comparison circuit using a current source and current mirror circuit. In FIG. 6, the same reference numerals as in FIG. 2 denote the same parts, and a detailed description thereof will be omitted.

The current mirror circuit 25 is comprised of n-channel MOS transistors 28 and 29. The drain and gate of the MOS transistor 28 are connected to the output terminal of the circuit unit 23 (which is equivalently illustrated by current sources 23A and 23B in FIG. 6), and the source is connected to ground V_{SS}. The drain of the MOS transistor 29 is connected to the other terminal of the resistor 26, its source is connected to ground V_{SS}, and its gate is commonly connected to the gate of the MOS transistor 28.

FIG. 7 shows an arrangement example of the comparators (differential amplifiers) 27, 31, and 41 in the circuits shown in FIGS. 2, 3, 4, and 6. Each comparator is comprised of p-channel MOS transistors 61

to 64 and n-channel MOS transistors 65 to 67. The sources of the MOS transistors 61 and 62 which operate as a differential input pair are commonly connected, and their gates are respectively connected to differential input terminals 68 and 69 which operate as an inverting input terminal (-) and non-inverting input terminal (+). The drain-source path of the MOS transistor 63 is connected between the power supply V_{DD} and the common source connection node between the MOS transistors 61 and 62. The drains of the MOS transistors 61 and 62 are commonly connected to those of the MOS transistors 65 and 66. The gates of the MOS transistors 65 and 66 are commonly connected to the drain of the MOS transistor 65; and their sources, to ground V_{SS}.

The source of the MOS transistor 64 is connected to the power supply V_{DD}, its drain is connected to an output terminal 70, and its gate is commonly connected to its drain and the gate of the MOS transistor 63. The drain of the MOS transistor 67 is connected to the output terminal 70; its source, to ground V_{SS}; and its gate, to the common drain connection node between the MOS transistors 62 and 66.

The comparator having this arrangement amplifies signals input to the differential input terminals 68 and 69 by the MOS transistors 61, 62, 65, and 66, and further amplifies the signals by the MOS transistors

63, 64, and 67. The comparator can operate even by a low-potential input signal.

FIG. 8 shows a circuit, e.g., latch circuit which is reset by the power-on reset circuit shown in FIGS. 2 to 7. The latch circuit is a flip-flop comprised of a 2-input NAND gate 71 and 3-input NAND gate 72. The flip-flop latches data on the basis of signals input to a set terminal S and reset terminal R, and obtains an output signal Q. Upon power-on, the flip-flop receives the power-on detection signal PDS and is initialized.

FIG. 9 shows changes along the time axis in the potential of the power supply V_{DD} upon power-on, the level of the power-on detection signal PDS, and the voltages V1 and V2. After power-on, the potential of the power supply V_{DD} rises. On the initial stage of power-on, the voltage V2 is higher than V1. When the potential of the power supply V_{DD} reaches a circuit operable level, the voltage V1 becomes higher than V2. Accordingly, the level of the power-on detection signal PDS which rises similarly to the potential of the power supply V_{DD} is inverted from "H" level to "L" level. As the potential of the power supply V_{DD} further rises, the voltage V2 becomes higher than V1. The power-on detection signal PDS output from the comparator 27 is inverted to "H" level, and power-on is detected.

In this arrangement, the BGR circuit 20 is used to generate the voltages V1 and V2 free from temperature

dependency. The voltages V1 and V2 are compared to generate the power-on detection signal PDS. The temperature dependency can be substantially eliminated. The circuit is constituted using a pair of MOS transistors, eliminating the influence of process variations. By controlling the resistance value of the resistor 53, the power-on detection level can be freely adjusted.

FIG. 10 is a circuit diagram for explaining a power-on detector and power-on reset circuit according to the second embodiment of the present invention. This circuit comprises comparators 81 to 83, p-channel MOS transistors 84 to 90, n-channel MOS transistors 91 and 92, resistors 93 to 96, and diodes 97 and 98.

The source of the MOS transistor 84 is connected to a power supply V_{DD}; its drain, to the non-inverting input terminal (+) of the comparator 81; and its gate, to the output terminal of the comparator 81. One terminal of the resistor 93 is connected to the drain of the MOS transistor 84; and the other terminal, to the anode of the diode 97. The cathode of the diode 97 is connected to ground V_{SS}. The source of the MOS transistor 85 is connected to the power supply V_{DD}; its drain, to the inverting input terminals (-) of the comparators 81 and 82; and its gate, to the output terminal of the comparator 81. The anode of the diode 98 is connected to the drain of the MOS transistor 85;

and its cathode, to ground V_{SS}.

The source of the MOS transistor 86 is connected to the power supply V_{DD}; its drain, to the non-inverting input terminal (+) of the comparator 82; and its gate, to the output terminal of the comparator 82. One terminal of the resistor 94 is connected to the drain of the MOS transistor 86; and the other terminal, to ground V_{SS}.

The source of the MOS transistor 87 is connected to the power supply V_{DD}; and its gate, to the output terminal of the comparator 81. The source of the MOS transistor 88 is connected to the power supply V_{DD}, its drain is commonly connected to the drain of the MOS transistor 87, and its gate is connected to the output terminal of the comparator 82. The resistor 95 is connected between ground V_{SS} and the common drain connection node between the MOS transistors 87 and 88. The common drain connection node is connected to the inverting input terminal (-) of the comparator 83.

The source of the MOS transistor 89 is connected to the power supply V_{DD}; and its gate, to the output terminal of the comparator 81. The source of the MOS transistor 90 is connected to the power supply V_{DD}, its drain is commonly connected to the drain of the MOS transistor 89, and its gate is connected to the output terminal of the comparator 82. The drain and gate of the MOS transistor 91 are connected to the common drain

connection node between the MOS transistors 89 and 90. The source of the MOS transistor 91 is connected to ground V_{SS}.

One terminal of the resistor 96 is connected to the power supply V_{DD}; and the other terminal, to the drain of the MOS transistor 92 and the non-inverting input terminal (+) of the comparator 83. The source of the MOS transistor 92 is connected to ground V_{SS}; and its gate, to the gate of the MOS transistor 91. A power-on detection signal is output from the output terminal of the comparator 83.

The comparators 81 to 83 can reliably operate even at a low voltage around 1 V with the same arrangement as that of the circuit shown in FIG. 7.

In this arrangement, the basic arrangement and operation are the same as those in the first embodiment. More specifically, a BGR circuit is used to generate voltages V1 and V2 free from temperature dependency. The voltages V1 and V2 are compared to generate the power-on detection signal PDS. The temperature dependency can be substantially eliminated. By controlling the resistance value of the resistor 95 and 96 the power-on detection level can be freely adjusted.

In the second embodiment, the MOS transistor 85 and diode 98 are shared between the comparators 81 and 82. The output voltages V_{OUTA} and V_{OUTB} of the

comparators 81 and 82 are respectively received by a pair of MOS transistors 87 and 88 and a pair of MOS transistors 89 and 90. This can further reduce variations in manufacturing process.

The power-on detector having the above arrangement, and the power-on reset circuit using the power-on detector can suppress variations in power-on detection level caused by a temperature change or manufacturing variations, and can perform reliable detection operation or reset operation even at a low voltage.

In the power-on detector and power-on reset circuit according to the first and second embodiments, the conductivity types of each p-channel MOS transistor and each n-channel MOS transistor can be reversed, and the polarities of the power supplies V_{DD} and V_{SS} can be reversed.

As described above, according to one aspect of this invention, a power-on detector capable of suppressing variations in power-on detection level caused by a temperature change or manufacturing variations, and performing reliable detection operation even at a low voltage, and a power-on reset circuit using the power-on detector can be obtained.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details and representative embodiments

shown and described herein. Accordingly, various modifications may be made without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.